REMARKS

Claims 1-41 are currently pending. Claims 1, 6, 11, 19, 29 and 33 have been amended, without acquiescence or prejudice to pursue the original claims in a related application. No new matter has been added.

Rejections Under 35 U.S.C. § 102

Claims 1-41 were rejected under 35 U.S.C. § 102(b) as being anticipated by Lee et al., U.S. Patent No. 6,430,731 (hereinafter "Lee"). Applicant respectfully traverses.

Independent claim 1 recites the following limitations (emphasis added):

> determining at least a plurality of different arrival times and a plurality of different slews from **a plurality of timing events propagated to an input of a gate** based on a timing model of the gate;
>
> **selecting one of the plurality of timing events propagated to the input of the gate as a worst case timing event** based on at least **a combination of the gate's characteristics, an arrival time in the plurality of different arrival times and a slew in the plurality of different slews** of the plurality of timing events; and
>
> storing information related to the worst-case timing event.

Applicant respectfully submits that Lee fails to disclose each and every limitation of the present claims in a manner as recited therein.

Lee is directed to methods and apparatus for performing slew dependent signal bounding for signal timing analysis. Lee discloses signal timing analysis with respect to a circuit having at least one gate. In one aspect, Lee includes the step of determining a first constraint slew sensitivity value and a second constraint slew sensitivity value for the at least one gate according to a specified bounding technique. Then, a ***representative signal*** for the gate is ***computed*** in accordance with the first and second values including an ***arrival time and slew rate***, wherein the representative signal bounds signal paths by bounding a maximum slew sensitivity path and a minimum slew sensitivity path. ***Such a representative signal may be computed for a worst case late-mode analysis and/or a best case early-mode analysis.***

Specifically, Lee discloses in step 150 and 160 in column 15 lines 44-48 a calculated representative signal and not an actual signal.

> Signals ***representing*** the ***arrival time and slew*** are ***computed*** at the gate output according to equations (1) and (2) above. Then, in step 160, the ***representative*** signal (s, a) is ***computed*** with the arrival time and slew according to equation (26) above. (Emphasis added)

Thus, Lee **calculates** the worse case timing event and does **not** include **selecting** a timing event propagated to the input of the gate based on a combination of the gate's characteristics, an arrival time and a slew as claimed.

Lee merely calculates a representative signal for a gate using arrival time and skew. Lee is silent with respect to using a combination of **the gate's characteristics**, arrival time and skew as claimed. For at least these reasons, it is respectfully submitted that independent claim 1 is not anticipated by the Lee reference.

For at least these same reasons, it is respectfully submitted that independent claims 6, 11, 19, 29 and 33 are likewise not anticipated by the cited references because they recite a limitation substantially similar to the limitation identified discussed with respect to claim 1 .

Since the remaining claims depend from these independent claims 1, 6, 11, 19, 29 and 33, respectively, these remaining dependent claims are also not anticipated and are therefore allowable over the cited references for the same reasons discussed above with respect to claim 1.

CONCLUSION

Based on the foregoing, all claims are believed allowable, and an allowance of the claims is respectfully requested. If the Examiner has any questions or comments, the Examiner is respectfully requested to contact the undersigned at the number listed below.

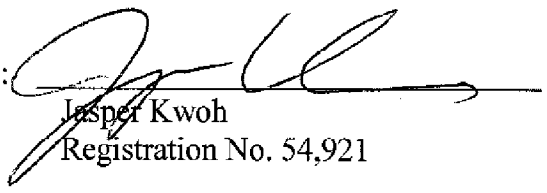
To the extent that any arguments and disclaimers were presented to distinguish prior art, or for other reasons substantially related to patentability, during the prosecution of any and all parent and related application(s)/patent(s), Applicant(s) hereby explicitly retracts and rescinds any and all such arguments and disclaimers, and respectfully requests that the Examiner re-visit the prior art that such arguments and disclaimers were made to avoid.

Credit card payment by USPTO - EFS in the amount of $810.00 is charged herein.

The Commissioner is authorized to charge Vista IP Law Group LLP Account No. 50-1105 for any fees required that are not covered, in whole or in part, and to credit any overpayments to said Deposit Account No. 50-1105.

Respectfully submitted,

Dated: June 17, 2008

By: 
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